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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,346	07/18/2003	Sachio Ogawa	61282-032	2580

7590 09/07/2004

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EXAMINER	
TANG, MINH NHUT	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,346	OGAWA, SACHIO	
	Examiner	Art Unit	
	Minh N. Tang	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 6* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement filed July 18, 2003 fails to comply with 37 CFR 1.98(a)(1), which requires a list of all patents, publications, or other information submitted for consideration by the Office. It has been placed in the application file, but the information referred to therein has not been considered.

Drawings

3. The drawings are objected to because reference number "404" in the right of Fig. 4 should be -- 405 --. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct

any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. Figure 7 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

6. Claim 6 is objected to because of the following informalities:

a/ "the multichip module" (line 2) should be -- a multichip module --.

b/ "each being" (line 3) should be -- each said plurality of semiconductor chips being --.

c/ "the multichip module input/output cell" (line 5) should be -- the multichip module --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-3 and 5-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Whetsel (U.S.P. 6,728,915).

As to claim 1, Whetsel discloses, in Fig. 6, a multichip module (see column 1, lines 19-20, hereinafter MCM) comprising a plurality of semiconductor chips (604, 606) mounted on said multichip module (MCM), wherein each said plurality of semiconductor chips (604, 606) includes at least a plurality of input/output cells (608, 612) connected to a plurality of respective external terminals (626) of the multichip module (MCM), and testing means (602) for optionally setting states (i.e., test mode, functional mode) of said plurality of input/output cells (608, 612).

As to claim 2, Whetsel discloses in Fig. 6, said test means (602) controls all the states (test mode, functional mode) of said plurality of input/output cells (608, 612) that are commonly connected to the same external terminals (626).

As to claim 3, Whetsel discloses in Fig. 6, said test means (602) controls all the states (test mode, functional mode) of said plurality of input/output cells (608, 612) of the semiconductor chips (604, 606).

As to claim 5, Whetsel discloses, in Fig. 6, a multichip module (see column 1, lines 19-20, hereinafter MCM) comprising a plurality of semiconductor chips (604, 606) mounted on said multichip module (MCM), wherein each said plurality of semiconductor chips (604, 606) includes at least a plurality of input/output cells (D0, D31) connected to a plurality of respective external terminals (626) of the multichip module (MCM) with being subjected to a boundary scan design, and boundary scan means (608, 612) mounted on said plurality of semiconductor chips (604, 606) for optionally setting states (i.e., test mode, functional mode) of said plurality of input/output cells (D0, D31).

As to claim 6, Whetsel discloses, in Fig. 6, a multichip module testing method of carrying out a burn-in test for a multichip module (see column 1, lines 19-20, hereinafter MCM) which is provided with a plurality of semiconductor chips (604, 606) thereon, each said plurality of semiconductor chips (604, 606) being provided with at least a plurality of input/output cells (608, 612) connected to a respective plurality of external terminals (626) of the multichip module (MCM), comprising the steps of: toggling an input/output control signal to one of said plurality of input/output cells (see column 5, line 43 to column 6, line 18) connected to one of said plurality of external terminals (626) which is not shared by said plurality of semiconductor chips (604, 606); and toggling an input/output control signal (see column 5, line 43 to column 6, line 18) with exclusively controlling a state thereof, said respective plurality of external terminals (626) being shared by said plurality of semiconductor chips (604, 606).

Allowable Subject Matter

9. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 4 recites, inter alia, said test means includes: a first sets of plural flip-flops of which configuration is based on that of a shift register; a second sets of plural flip-flops of which inputs are connected to corresponding outputs of the first sets of plural flip-flops; and a selector for selecting a normal signal in a non-test mode, while selecting an output from the second sets of flip-flops in a test mode, so as to give an input/output control signal to said plurality of input/output cells.

The art of record does not disclose the above limitations, nor would it be obvious to modify the art of record so as to include the above limitations.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Gruetzner et al.	5,444,715	AC Interconnect Test Of Integrated Circuit Chips.
Lee	5,581,176	Analog Autonomous Test Bus Framework For Testing Integrated Circuits On A Printed Circuit Board.
Hashizume	5,646,422	Semiconductor Integrated Circuit Device.
Tsuda	6,630,744	Multichip Module.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (571) 272-1971. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Minh Tang

Minh N. Tang
Primary Examiner
Art Unit 2829
8/31/04